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(54) Parallel output architectures for CMOS active pixel sensors

(57) An active pixel sensor formed by creating an X-Y array of pixels on a semiconductor substrate. The two dimensional array of pixels is arranged in a plurality of rows and columns that are addressed by addressing circuits formed on the substrate. The active pixel sensor is functionally divided to enable the addressing and reading out of a plurality of pixels simultaneously by providing areas, each of the areas having a row addressing circuit and a column addressing circuit. A signal processing circuit is provided for each area to output a sequential series of pixels in each of the areas. A correlated double sampling circuit is provided

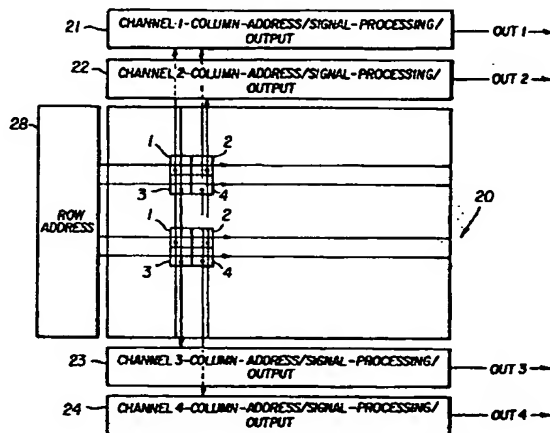


FIG. 2d

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Description

FIELD OF THE INVENTION

[0001] This invention relates generally to solid state imager sensors having multiple output channels, and more particularly to architectures based on CMOS active pixel sensors (APS) having multiple output channels that are designed for image capture requiring high frame and pixel rates. It is also applicable to systems where it is desirable to have separate output channels for each of the color defined by a mosaic Color Filter Array (CFA). The architecture is also suitable to other types of x-y addressable imaging array.

BACKGROUND OF THE INVENTION

[0002] The prior art has taught image sensors that have requirements to output data at a high pixel data rate. Typically, these high pixel rate requirements are achieved by employing a two-dimensional array (an x-y array) of pixels arranged into two split fields such that the output of one half of the pixels are sent to signal processing circuits located at an edge of the array adjacent to that half. The other half the pixels are output to similar circuits located adjacent to that half. Technologies that can be used to implement such arrays in the prior art have been CMOS APS or CCD. Other prior art teachings have disclosed two-dimensional arrays that are formed into many blocks that each having their own output paths. These multiple output path prior art devices have increased the output data rate for image sensor arrays, however, they are limited in the amount and types of versatility that they provide.

[0003] In a conventional CMOS APS, only a single row of the pixel array is addressed and the image data from that row is transferred in parallel to column circuits for signal processing such as offset removal. Each pixel in a selected row is read out in sequence to form one line of output image data. The total number of pixels in the array and the frame rate determine the pixel output rate. For high frame-rate devices or devices having a large pixel count for image capture, the data rate becomes excessive and the output channel electronics is no longer fast enough to capture and deliver the signal with high fidelity to the image digitization and store unit. For example, a 1000 x 1000 (megapixel) array running at 30 frames/second has a pixel output rate of over 30 MHz. However, a 500 x 500 pixel array running at 1000 frames/sec requires in excess of 250 MHz output data rate. Typical state-of-the-art pixel data channels (both the analog signal and the digitization circuits) are only capable pixel transfer rates in the of 10's of MHz range, and therefore multiple parallel output channels are necessary to achieve high pixel output rate for high frame rate and high pixels count sensors.

[0004] From the foregoing discussion, it should be apparent that there remains a need within the art for a

more versatile multiple array for achieving high pixel rate data transfers.

SUMMARY OF THE INVENTION

[0005] The present invention addresses the foregoing problems in the prior art by providing a CMOS based architecture for active pixel sensors (APS). A semiconductor substrate having a two dimensional array of pixels arranged in a plurality of rows and columns is provided with a row addressing circuit formed on the substrate, a column addressing circuit formed on the substrate, a plurality of signal processing circuits operatively connected to the array of pixels such that each of the signal processing circuits is electrically connected to a predetermined subset of pixels within the array through electrically conductive signal busses, wherein each of the subsets comprises a plurality of pixels, and means for employing the row addressing circuit and the column addressing circuit to select a sequence of pixels having one pixel for each of the subsets and simultaneously transferring signals from each of the pixel sequences to the signal processing circuits.

ADVANTAGEOUS EFFECT OF THE INVENTION

[0006] The present invention in providing a CMOS based architecture that is fully compatible with the APS characteristics yields numerous advantages: it provides x-y addressability; sub-windowing and sub-sampling of the pixel array (to provide for example a higher frame rate with fewer pixels per frame); for color image sensors having mosaic Color Filter Arrays it provides a parallel channel connection scheme can be used to preserve the CFA pattern during sub-sampling; and for CFA-based color image sensors, each of the parallel channels can be used for a single color to simplify color signal processing (such as color-specific gain setting and digitization).

BRIEF DESCRIPTION OF THE DRAWINGS

[0007]

Fig. 1 is a block diagram of a prior art device having two output circuits;

Fig. 2a is a block diagram of an embodiment of the present invention having four output channels;

Fig. 2b is a block diagram of an embodiment of the present invention having four output channels;

Fig. 2c is a block diagram of an embodiment of the present invention having four output channels;

Fig. 2d is a block diagram of an embodiment of the present invention having four output channels where the four pixels simultaneously output on the channels are arranged in a mosaic pattern;

Fig. 2e is a block diagram of an embodiment of the column addressing signal processing circuits of the

present invention;

Fig. 3a is a block diagram of an embodiment of the present invention having eight output channels;

Fig. 3b is a block diagram of an embodiment of the present invention having eight output channels;

Fig. 4 is a block diagram illustrating the basic functional blocks in the output channels;

Fig. 5 is a schematic diagram of each of the output channels in the preferred embodiment as envisioned by the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0008] Fig. 1, which is a block diagram of a prior art sensor device wherein the sensor 100 is arranged such that there are two individual photosensing fields 119, 129. The sensor 100 illustrated is a charge coupled device (CCD). Fields 101, 102 each have a horizontal shift register 105, 106 that provides an output path for each of the field 101, 102. The sensor if effectively operated as two individual sensors, thereby doubling the pixel data transfer rate of sensors having only a single field or frame. To further increase pixel data transfer rates, prior art sensors have provided field 101 with output taps 121-127 that operate in conjunction with output 120 to remove charges that are currently being transferred through horizontal shift register 105. In a similar manner field 102 has output taps 131-137 that operate in conjunction with output 130 to remove charges that are currently being transferred through horizontal shift register 106. This yields a total of 8 outputs (130-137). The large number of outputs greatly increases the pixel data transfer rate which is essential for certain systems having high speed requirements. However, no random addressing capability is provided by such

[0009] The present invention envisions that by connecting multiple (two or more) rows or multiple pixels to signal processing circuits in parallel using signal busses, multiple output circuits, or channels, can be used to lower per channel data rate requirements (Figures 2a through 2d) for devices that have high data rate requirements overall. This multiple channel implementation is also applicable to color x-y addressable sensors where it is desirable to have separate output channels for each different color. As an example of separate output channels for each different color is that each of pixels 1, 2, 3 and 4 (in Figures 2a through 2d) are each configured to sense a different color (such as Bayer pattern having 2 green, 1 red and 1 blue channels). The column-wise output signal routing connects all the pixels of the same color filter covering to a color specific output channel.

[0010] Referring to Fig. 2a, which is a block diagram of the present invention having a pixel array 10 with four output channels out 1, out 2 out 3 and out 4, the selected pixels 1, 2, 3, and 4 are output simultaneously via four discrete signal processing circuits 11, 12, 13, and 14. As shown in this embodiment the four selected

pixels 1, 2, 3 and 4 are selected from a single row that is selected by row address circuit 18 for output. Four parallel channels are thus implemented where 4 pixels from a selected row are addressed and read out to 4 different circuit blocks. Row addressing circuits 18 are provided on chip as envisioned by the present invention. Column addressing circuits are provided on chip also, but as envisioned by the present invention, are part of the signal processing circuits 11, 12, 13 and 14. The row and column addressing circuits, are conventional circuits that are well known within the art of image sensors. The signal processing circuits 11, 12, 13 and 14 as well as the output circuits out 1, out 2 out 3 and out 4 (which will be discussed in more detail below) are essentially identical circuits that are repeated for each of the four channels with variation only for purposes of color. The present invention as envisioned by Fig. 2a will have each channel handle one quarter of the pixels with four pixels being simultaneously processed, one by each channel.

[0011] Fig. 2b is a block diagram of another embodiment of the present invention having four output channels that is a variation of the embodiment discussed in Fig. 2a. Referring to Fig. 2b, pixel array 20 with four output channels out 1, out 2 out 3 and out 4, simultaneously output the selected pixels 1, 2, 3, and 4 via four discrete, signal processing circuits 21, 22, 23, and 24. Here, two consecutive rows are required to select the four pixels that are being processed simultaneously by four different circuit blocks. The pixels as presented in the embodiment shown in Fig. 2b are, typically, part of a mosaic color filter array (CFA) pattern that are typically used within the prior art. As shown the four pixels that are processed in parallel are associated based on color, with two green pixels (indicated by G), one blue pixel (indicated by B) and one red pixel (indicated by R) four each group of four that are simultaneously processed.

[0012] Fig. 2c is a block diagram of another embodiment of the present invention having four output channels that is a variation of the previous embodiments that have been discussed. Pixel array 30 has four output channels out 1, out 2 out 3 and out 4, with the selected pixels 1, 2, 3, and 4 being output simultaneously via four discrete signal processing circuits 31, 32, 33, and 34. Fig. 2c is a block diagram illustrating a 4 channel variation where the signal processing circuits 31, 32, 33 and 34 are located on only one side of the imaging x-y array. The selected pixels 1, 2, 3 and 4 illustrated here are on consecutive rows, though not necessarily adjacent pixels preventing the formation a mosaic pattern. This is for illustrative purposes to show that a variety of schemes can be used in placement of the circuitry associated with the pixels selected for output.

[0013] Fig. 2d details the connection matrix of the selected pixels 1, 2, 3 and 4 to the color-specific channels within sensor 20 for the embodiment shown in Fig. 2b illustrating the column signal busses used to connect various pixels to output channels. As seen in Fig. 2d,

each column has at least two signal busses connecting half the pixels in that column to pixels in accordance with the channel that those pixels are associated with. Thus, half the columns have signal bus lines interfacing pixel types 1 and 3 with respective signal processing circuits 21, 23 and the other half have signal bus lines interfacing pixel types 2 and 4 with respective signal processing circuits 22, 24.

[0014] Fig. 2e details a block diagram for interfacing column signal bus lines with signal processing and column addressing circuits. Pixel data arrives from the pixel column bus into a CDS circuit 91 where double sampling takes place. A column select signal is applied to switches 95, 96 to alternately supply difference amplifier 92 with the reset sample and signal sample to provide an adjusted output for each of the columns that are currently selected by the column address circuit. Switches 95, 96 are transistor configurations that can be any of CMOS, PMOS or NMOS circuits, depending upon the design criteria that is employed by a given process. The difference amplifier 92 may have its gain value be a fixed value, or the gain value can be programmable. A programmable gain value can be provided either at the metal or at the logic level.

[0015] Another architecture is to divide the array into quadrants and then apply the same multiple-pixel connection architecture previously discussed to achieve even higher number of parallel channels. Fig. 3a is a block diagram of an embodiment of the present invention wherein the array is divided into four x-y array quadrants 41, 42, 43 and 44 that each have two output channels resulting in eight total output channels, with each output channel having its own column-address/signal processing output (51-58). The four x-y array quadrants 41, 42, 43 and 44 also each have their own individual row address circuits 81, 82, 83 and 84. The invention disclosed here allows the construction of parallel channels to enable either high frame rate or high pixel count image sensors. An 8-channel implementation of a 512 x 512 array of pixels is capable of transferring 1000 frames/sec resulting in channel data rate on the order of 35 MHz rate (depending on the overhead time involved in addressing, output setup time etc.) which is quite reasonable for incorporating per-column correlated double sampling (CDS) or per channel analog-to-digital conversion in each channel. Using the quadrant architecture (as seen in Fig. 3a) and double row output, the loss of pixel fill factor due to the addition of column signal busses (two per column) is minimal. A 16-channel imager can also be constructed by using four column signal busses to output the pixel signals to four parallel addressing/signal-processing/output circuit blocks attached to each imager quadrant.

[0016] Fig. 3b is a block diagram of an embodiment of the sensor having four x-y array quadrants 41, 42, 43 and 44 of present invention having eight output channels as shown in Fig. 3a however, in Fig. 3b the eight output channels are configured to have color specific

output channels. The preferred method of arranging output channels in a color specific manner is to employ row addressing techniques that sequences the reading out of adjacent color pixels simultaneously to different channels. The preferred process for design layout of the four x-y array quadrants 41, 42, 43 and 44 and their respective addressing and signal processing circuits shown in Figures 3a and 3b, is to form one of the four arrays with its respective addressing and signal processing circuits. The array is then mirrored a first time to create two quadrants with their associated addressing and signal processing circuits. The two quadrant mirrored design is then mirrored again to create the four quadrants 41, 42, 43 and 44. It should also be appreciated that the layout can design all four quadrants individually, and that such a layout will have somewhat different addressing characteristics that may simplify the signal processing. However, the preferred embodiment envisions that the simplicity of the mirrored design technique makes any additional signal processing to join the four quadrants worthwhile.

[0017] Fig. 4 is a block diagram illustrating the basic functional blocks used in the output channels. The output channels are essentially identical to one another, or at least very similar. Correlated double sampling (CDS) 91 is provided for each of the output channels previously discussed to provide the voltage level signal for each pixel. The preferred embodiment employs a difference amplifier with each of the correlated double sampling units 91 which in turn outputs an adjusted voltage to a programmable gain amplifier (PGA) 93 from each of the channels. The PGA 93 will provide a predetermined amount of gain for each of the channels which is typically based on color but can also be based on other factors.

[0018] Fig. 5 is a schematic diagram that generally applies to each of the output channels in the preferred embodiment as envisioned by the present invention. The CDS receives two samples (Reset and Signal) for each pixel, and accordingly provides two sample and hold circuits 101, 102, one for each the Reset and the Signal samples received from the associated pixel. Each the Reset and the Signal samples are stored on their associated capacitor C_S , C_R within the CDS 91 when their respective switches S, R are closed. The values stored on capacitors C_S and C_R are applied to the input of difference amplifier 95. These stored Signal and Reset samples are used as inputs to a difference amplifier. The difference amplifier outputs to a PGA which, in the preferred embodiment is a variable resistor on the difference amplifier output. It should be understood, that the PGA can excepts the output of the CDS and have a differential amplifier placed after the PGA, however the preferred embodiment places the differential amplifier immediately after the CDS. It should also be understood that the PGA can use as a variable gain element a transistor, a DAC or the like as well as a variable resistor. The CDS is reset by a transistor circuit that clears both

the Signal and the Reset capacitors. In the preferred embodiment PMOS transistors are used to clear the

[0019] Other aspects of the invention include: the sensor wherein each column is associated with a two subsets; the sensor wherein each column is associated with a plurality of the subsets and further comprising customization means for altering the association between pixels and subsets; the active pixel sensor further comprising a correlated double sampling circuit for each subset within the sensor; the active pixel sensor wherein the pixels in the array further comprises a pinned photodiode within each of the pixels; the active pixel sensor wherein the sensor is a CMOS sensor; the sensor wherein each column is associated with a single subset; the sensor wherein each column is associated with a two subsets; the active pixel sensor further comprising a correlated double sampling circuit for each subset within the sensor; the active pixel sensor wherein the pixels in the array further comprises a pinned photodiode within each of the pixels; and the active pixel sensor wherein the sensor is a CMOS sensor.

[0020] The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

PARTS LIST

[0021]

1	selected pixel
2	selected pixel
3	selected pixel
4	selected pixel
10	pixel array
11	signal processing circuit
12	signal processing circuit
13	signal processing circuit
14	signal processing circuit
18	row addressing circuit
20	pixel array
21	signal processing circuit
22	signal processing circuit
23	signal processing circuit
24	signal processing circuit
28	row addressing circuit
30	pixel array
31	signal processing circuit
32	signal processing circuit
33	signal processing circuit
34	signal processing circuit
38	row addressing circuit
41	pixel array
42	pixel array
43	pixel array
44	pixel array

51	signal processing circuit
52	signal processing circuit
53	signal processing circuit
54	signal processing circuit
5 55	signal processing circuit
56	signal processing circuit
57	signal processing circuit
58	signal processing circuit
81	row addressing circuit
10 82	row addressing circuit
83	row addressing circuit
84	row addressing circuit
90	signal processing circuit
91	correlated double sampling unit
15 92	difference amplifier
93	programmable gain amplifier
95	switch
96	switch
101	reset sample circuit
20 102	signal sample circuit
100	prior art sensor
119	field
120	output
121	output
25 122	output
123	output
124	output
125	output
126	output
30 127	output
129	output
130	output
131	output
132	output
35 133	output
134	output
135	output
136	output
137	output
40 129	field
C _R	Reset storage capacitor
C _S	Signal storage capacitor
R	Reset switch
S	Signal switch

Claims

1. An active pixel sensor comprising:

50	a semiconductor substrate having a two dimensional array of pixels arranged in a plurality of rows and columns;
	a row addressing circuit formed on the substrate;
55	a column addressing circuit formed on the substrate;
	a plurality of signal processing circuits operatively connected to the array of pixels such that

each of the signal processing circuits is electrically connected to a predetermined subset of pixels within the array through electrically conductive signal busses, wherein each of the subsets comprises a plurality of pixels; and means for employing the row addressing circuit and the column addressing circuit to select a sequence of pixels having one pixel for each of the subsets and simultaneously transferring signals from each of the pixel sequences to the signal processing circuits.

2. The sensor of claim 1 wherein the sensor is a color sensor and the each of the subsets represent a single color.

3. The sensor of claim 1 wherein each column is associated with a single subset.

4. The active pixel sensor of claim 1 wherein the array is functionally divided into a plurality of areas, each of the areas having a row addressing circuit and a column addressing circuit.

5. The active pixel sensor of claim 4 wherein each of the columns has a plurality of signal busses such that each of the signal busses corresponds to one of the signal processing channels.

6. An active pixel sensor comprising:

a semiconductor substrate having a two dimensional array of pixels arranged in a plurality of rows and columns;

a row addressing circuit formed on the substrate;

a column addressing circuit formed on the substrate;

a plurality of signal processing circuits operatively connected to the array of pixels such that each of the signal processing circuits is electrically connected to a predetermined subset of pixels within the array through electrically conductive signal busses, wherein each of the subsets comprises a plurality of pixels;

means for employing the row addressing circuit and the column addressing circuit to select a sequence of pixels having one pixel for each of the subsets and simultaneously transferring signals from each of the pixel sequences to the signal processing circuits; and

wherein the array is functionally divided into a plurality of areas, each of the areas having a row addressing circuit and a column addressing circuit and each of the areas further being a mirror image of one of the other areas.

7. The active pixel sensor of claim 6 wherein each of

the columns has a plurality of signal busses such that each of the signal busses corresponds to one of the signal processing channels.

8. The sensor of claim 6 wherein the sensor is a color sensor and the each of the subsets represent a single color.

9. The sensor of claim 6 wherein each column is associated with a plurality of the subsets and further comprising customization means for altering the association between pixels and subsets.

10. A method for forming an active pixel sensor comprising:

providing a semiconductor substrate having a two dimensional array of pixels arranged in a plurality of rows and columns formed on the substrate, with a row addressing circuit that can address each of the rows, a column addressing circuit that can address each of the columns, and at least one signal processing circuit that is operatively connected to the array of pixels such that each of the signal processing circuits is electrically connected to a predetermined subset of pixels within the array through electrically conductive signal busses, wherein each of the subsets comprises a plurality of pixels; and mirroring the two dimensional array, its associated row and column addressing circuit, and its signal processing circuit to create a second x-y array that is the mirror image of the first x-y array.

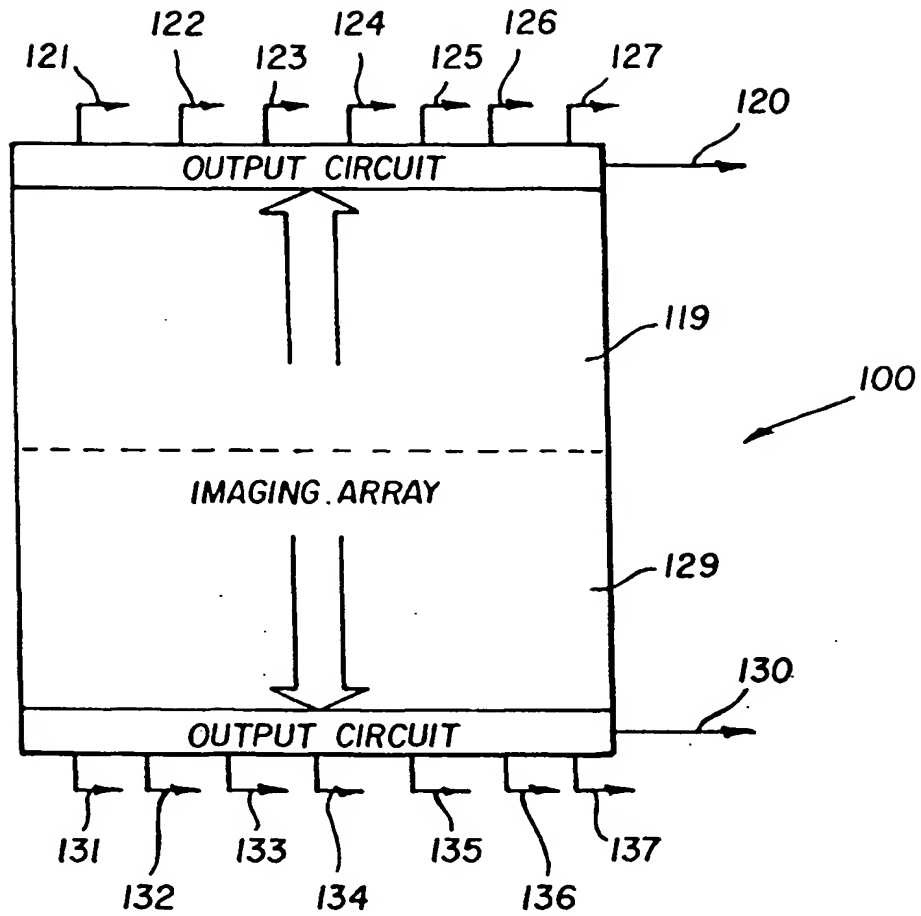


FIG. 1

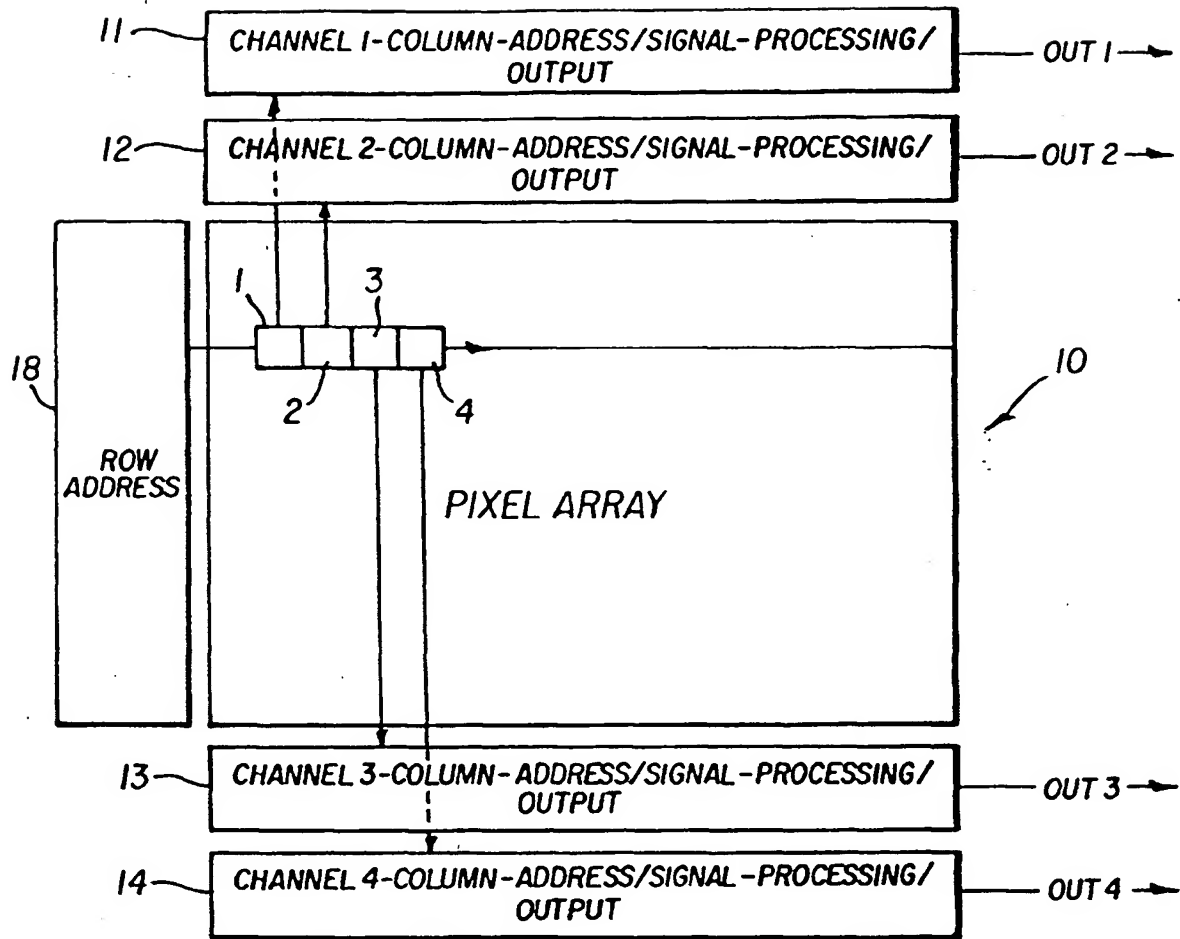


FIG. 2a

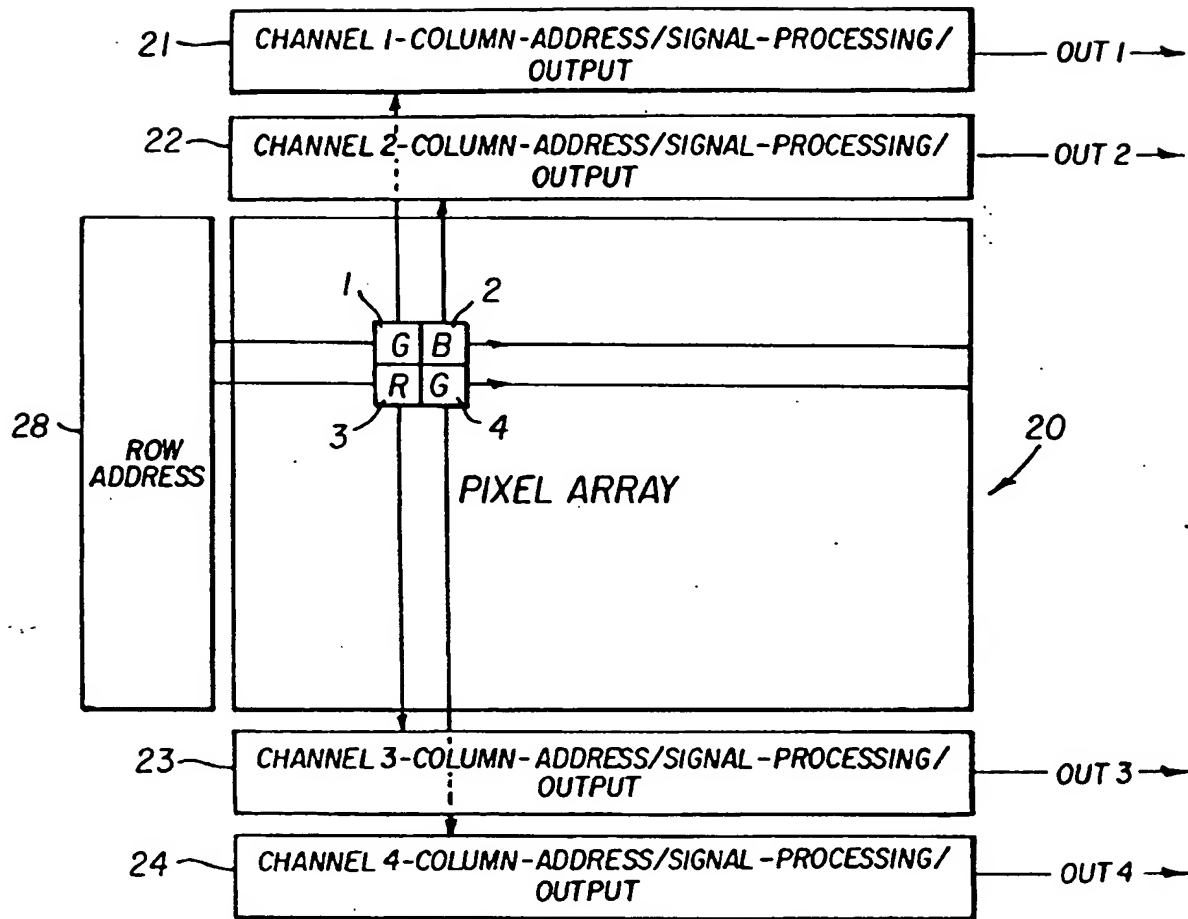


FIG. 2b

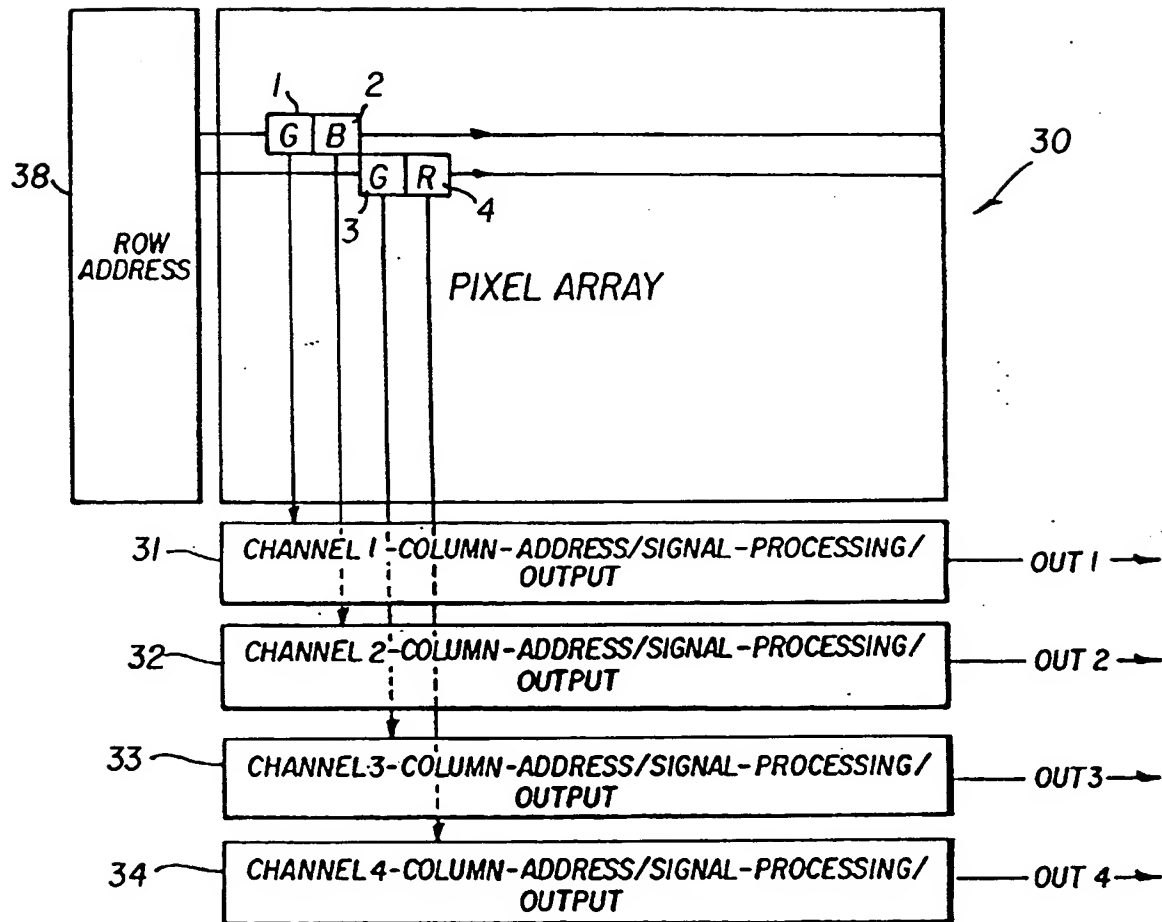


FIG. 2c

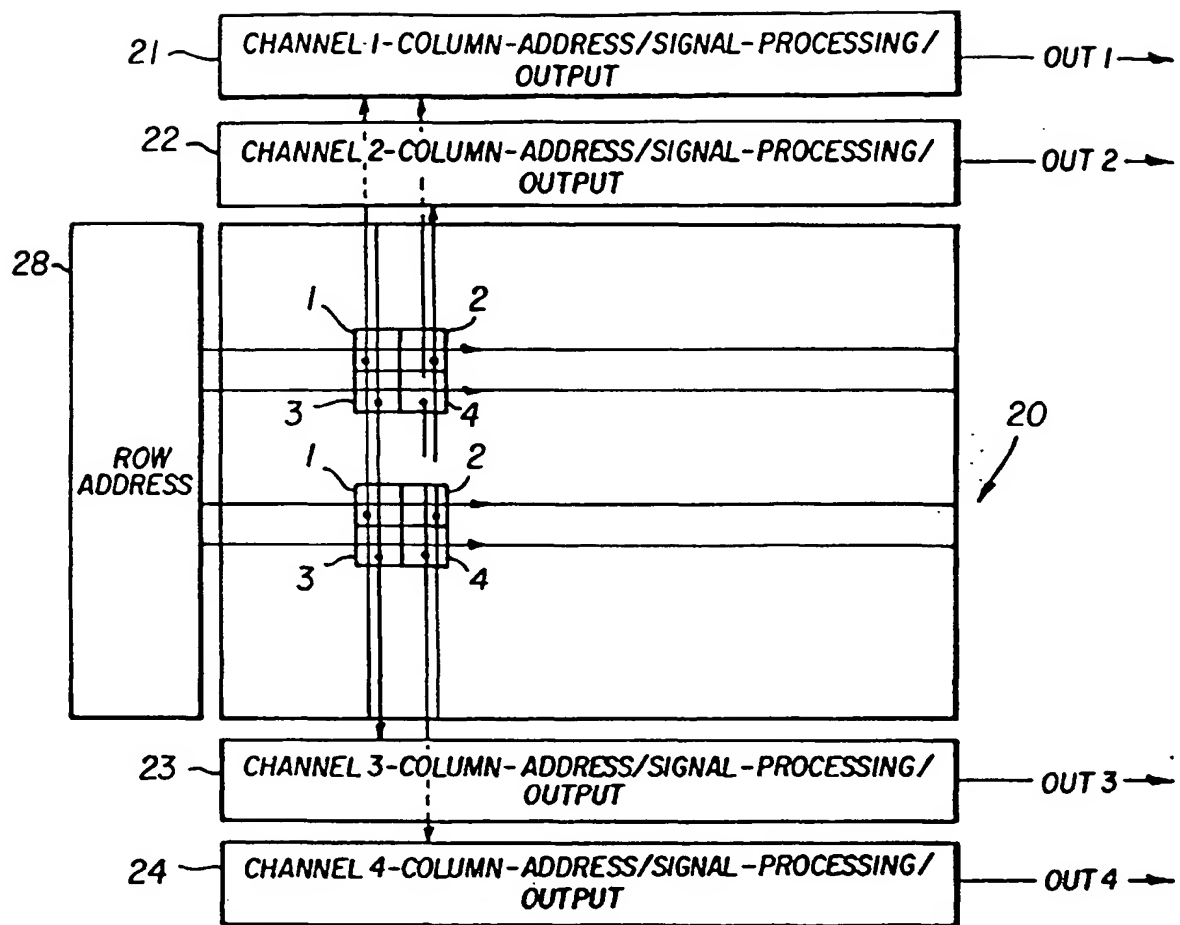


FIG. 2d

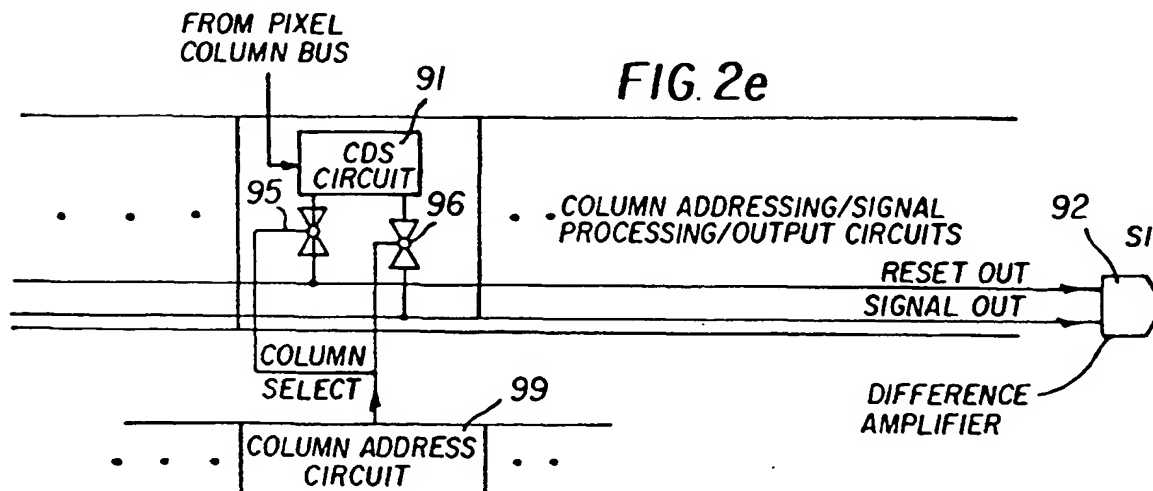


FIG. 2e

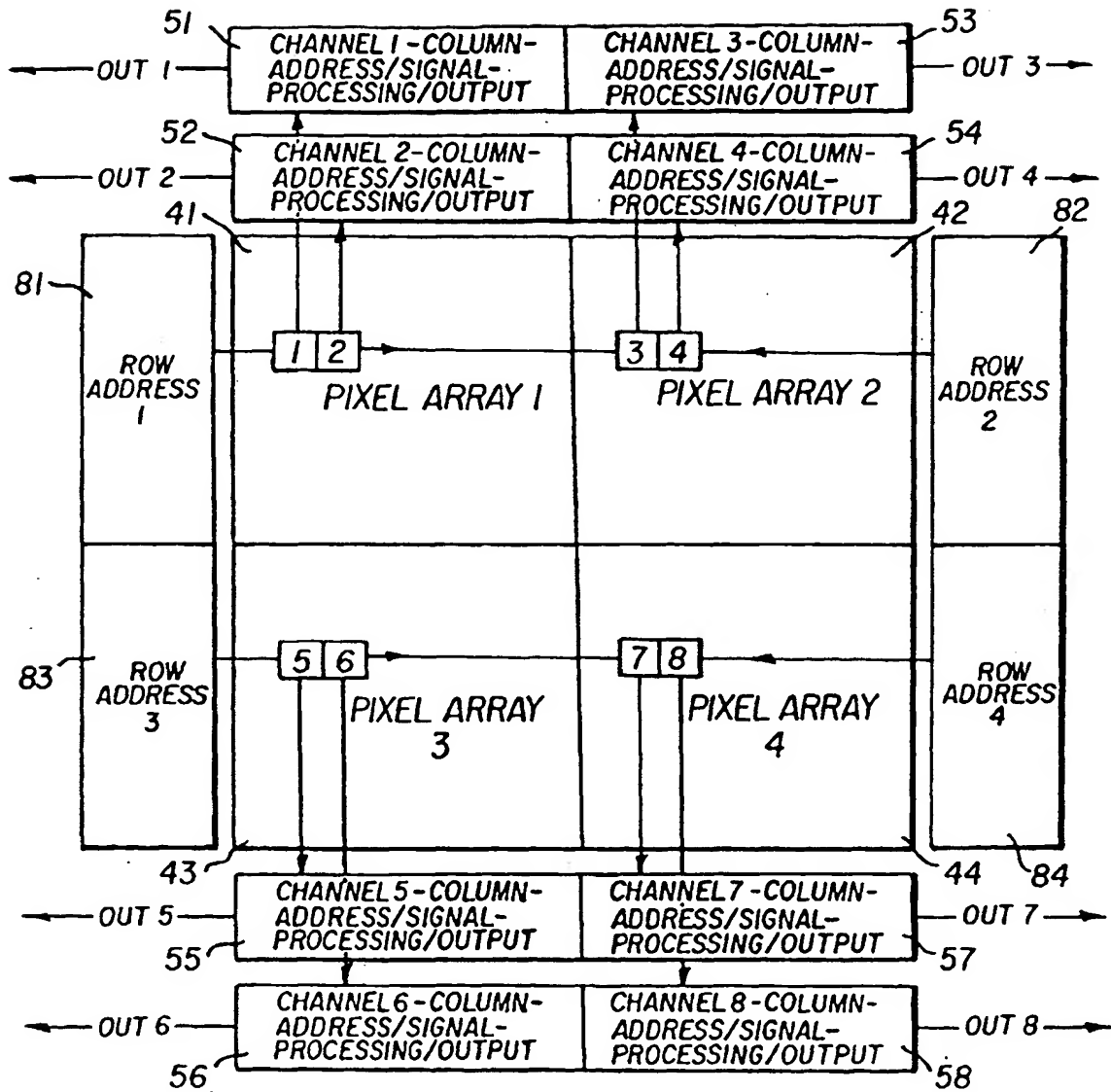


FIG. 3a

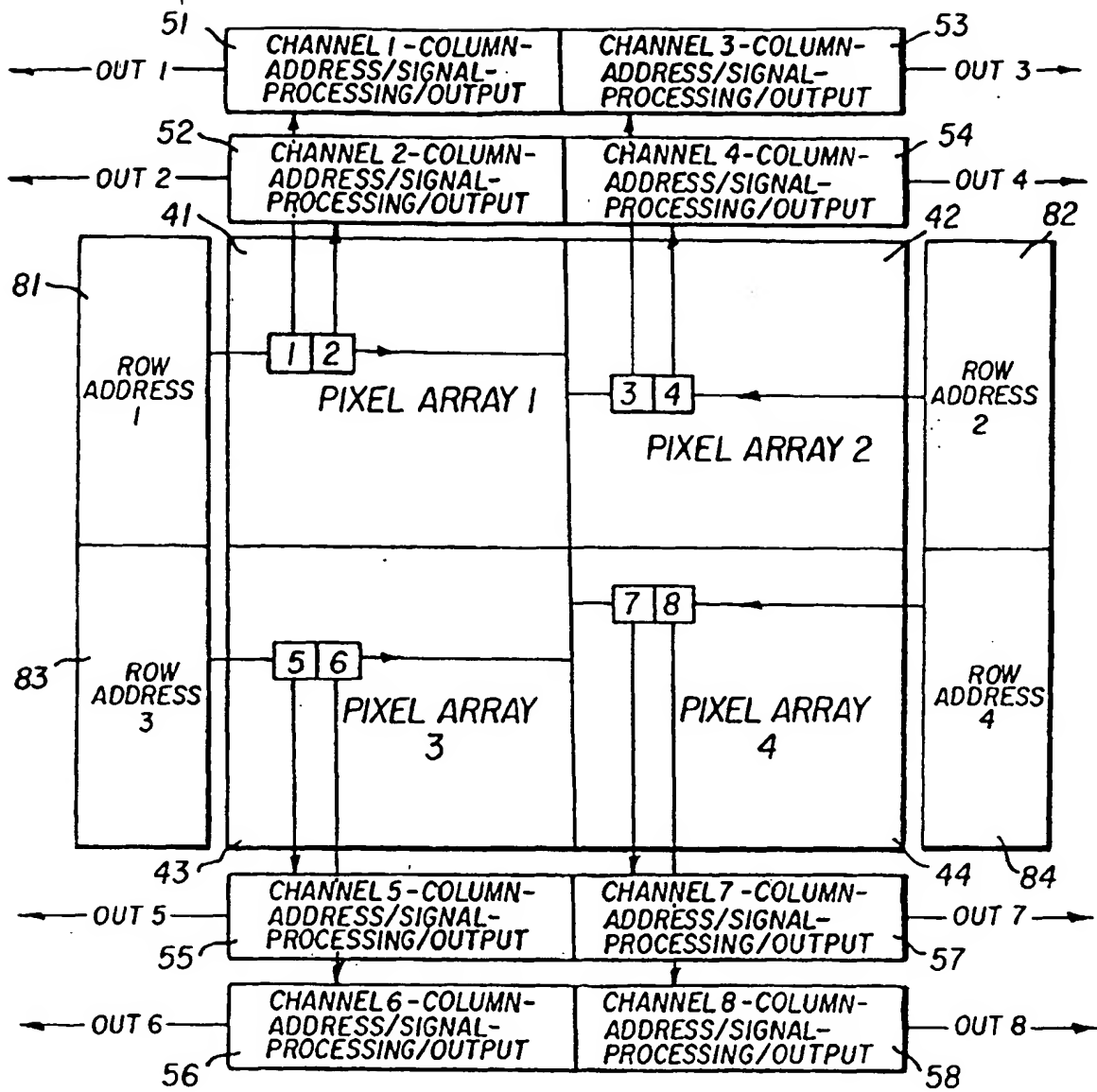
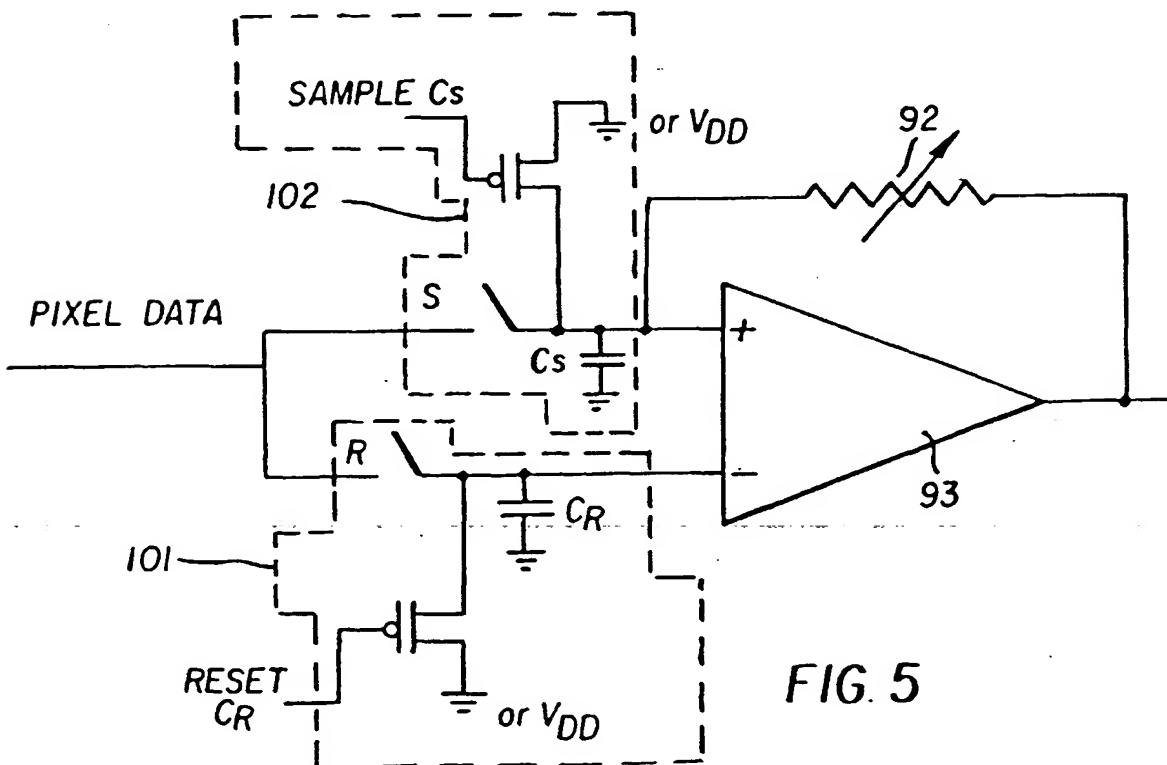
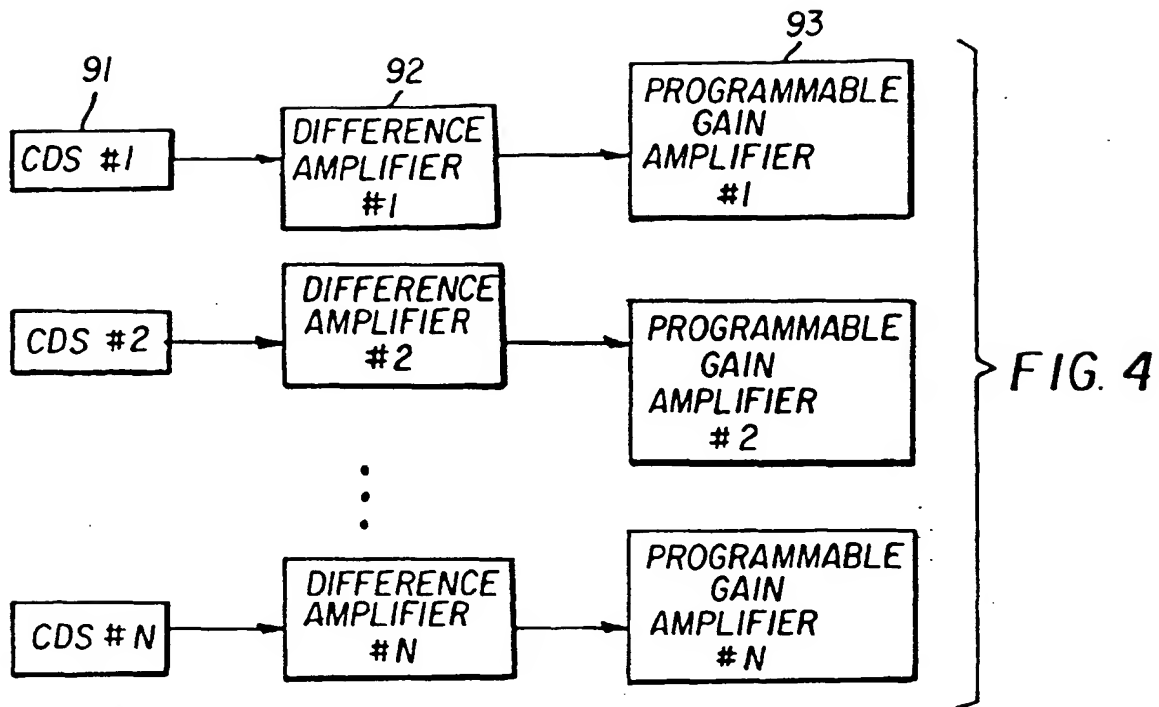


FIG. 3b



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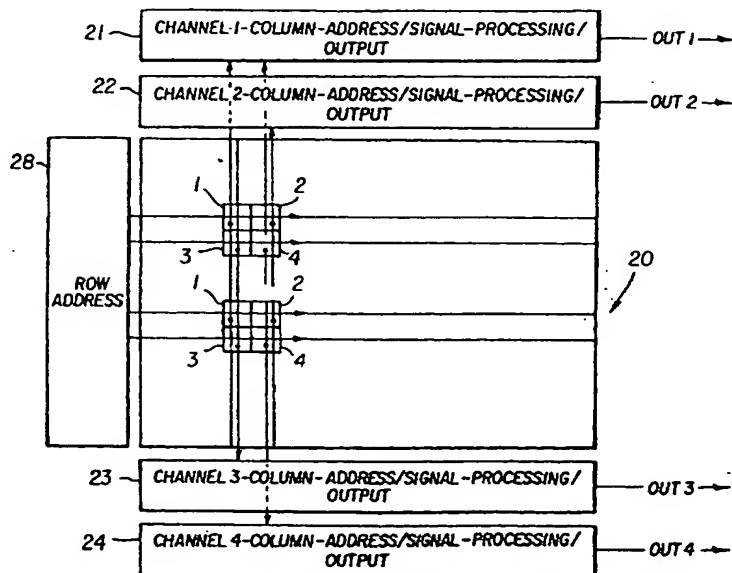


FIG. 2d

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European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 99 20 1836

DOCUMENTS CONSIDERED TO BE RELEVANT			
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			H04N
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 13 May 2002	Examiner De Paepé, W
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
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**ANNEX TO THE EUROPEAN SEARCH REPORT
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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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